REMARKS

Claims 1-22 are pending. Claims 1, 9 and 16-17 are amended herein. No new matter is added as a result of the claim amendments.

The Examiner has indicated that Claims 6-7, 14-15 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant thanks the Examiner for indicating the allowability of Claims 6-7, 14-15 and 18-20.

112 Rejections

The instant Office Action states that Claims 1-22 are rejected under 35 U.S.C. § 112, second paragraph, because the term "can be" in independent Claims 1, 9 and 17 is indefinite. Applicant respectfully submits that Claims 1, 9 and 17, as amended herein, and consequently the claims dependent on Claims 1, 9 and 17, overcome the rejection under 35 U.S.C. § 112, second paragraph

102 Rejections

The instant Office Action states that Claims 1, 3, 5, 9, 11 and 13 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ryan et al. ("Ryan;" U.S. Patent No. 6,311,149). The Applicant has reviewed the cited reference and respectfully submits that the present invention as recited in Claims 1, 3, 5, 9, 11 and 13 is not shown or suggested by Ryan.

Applicant respectfully submits that Ryan does not show or suggest "A multi-functional device comprising: a bus; a random access memory (RAM) coupled to said bus; a central processing unit (CPU) coupled to said bus; and a plurality of analog blocks coupled to said bus, wherein said bus, RAM, CPU and analog blocks reside on a single chip" as recited in independent Claim 1 (emphasis added). Claims 3 and 5 are dependent on Claim 1 and recited additional limitations.

Also, Applicant respectfully submits that Ryan does not show or suggest "A method for implementing multiple functions in a device, said method comprising selecting a first analog block from a plurality of analog blocks coupled to a bus, a random access memory and a central processing unit on a single chip" as recited in independent Claim 9 (emphasis added). Claims 11 and 13 are dependent on Claim 9 and recite additional limitations.

Therefore, Applicant respectfully submits that Ryan does not show or suggest the claimed features of the present invention as recited in independent Claims 1 and 9, and that these claims are in condition for allowance. Applicant also respectfully submits that Ryan does not show or suggest the additional claimed features of the present invention as recited in Claims 3 and 5 dependent on Claim 1, and Claims 11 and 13 dependent on Claim 9, and that Claims 3, 5, 11 and 13 are in condition for allowance as being dependent on allowable base claims. As such, the Applicant respectfully asserts that the basis for rejecting Claims 1, 3, 5, 9, 11 and 13 under 35 U.S.C. § 102(e) is traversed.

103 Rejections

Claims 8, 16 and 22

The instant Office Action states that Claims 8, 16 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryan. The Applicant has reviewed the cited reference and respectfully submits that the present invention as recited in Claims 8, 16 and 22 is not shown or suggested by Ryan.

Claim 8 is dependent on independent Claim 1 and recites additional limitations. Claim 16 is dependent on independent Claim 9 and recites additional limitations. As presented above, Applicant respectfully submits that Ryan does not show or suggest the present invention as recited in Claims 1 and 9.

Claim 22 is dependent on independent Claim 17 and recites additional limitations. Independent Claim 17 recites that an embodiment of the present invention is directed to "An array of analog blocks comprising: a first plurality of analog blocks...; and a second plurality of analog blocks ..., and wherein said first plurality and second plurality of analog blocks are coupled to a bus, a random access memory and a central processing unit on a single chip" (emphasis added). Applicant respectfully submits that Ryan does not show or suggest the limitations of Claim 17.

In summary, Applicant respectfully submits that Ryan does not show or suggest the claimed features of the present invention as recited in

independent Claims 1, 9 and 17. As such, Applicant also respectfully submits that Ryan does not show or suggest the additional claimed features of the present invention as recited in Claims 8, 16 and 22, and that Claims 8, 16 and 22 are in condition for allowance as being dependent on allowable base claims. As such, the Applicant respectfully asserts that the basis for rejecting Claims 8, 16 and 22 under 35 U.S.C. § 103(a) is traversed.

Claims 2 and 10

The instant Office Action states that Claims 2 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryan in view of either Anderson (U.S. Patent No. 5,493,246) or Swanson (U.S. Patent No. 6,590,517). The Applicant has reviewed the cited references and respectfully submits that the present invention as recited in Claims 2 and 10 is not shown or suggested by Ryan and Anderson or Swanson, alone or in combination.

Claim 2 is dependent on Claim 1 and recites additional limitations. Claim 10 is dependent on Claim 9 and recites additional limitations. As presented above, Applicant respectfully submits that Ryan does not show or suggest the present invention as recited in Claims 1 and 9.

Applicant respectfully submits that Anderson does not overcome the shortcomings of Ryan. Specifically, Applicant respectfully submits that Anderson, alone or in combination with Ryan, does not show or suggest "A multi-functional device comprising: a bus; a random access memory (RAM) coupled to said bus; a central processing unit (CPU) coupled to said

bus; and a plurality of analog blocks coupled to said bus, wherein said bus, RAM, CPU and analog blocks reside on a single chip" as recited in independent Claim 1, nor does Anderson, alone or in combination with Ryan, show or suggest "A method for implementing multiple functions in a device, said method comprising selecting a first analog block from a plurality of analog blocks coupled to a bus, a random access memory and a central processing unit on a single chip" as recited in independent Claim 9.

Also, Applicant respectfully submits that Swanson does not overcome the shortcomings of Ryan. Specifically, Applicant respectfully submits that Swanson, alone or in combination with Ryan, does not show or suggest the limitations of Claims 1 and 9 cited above.

Therefore, Applicant respectfully submits that Ryan and Anderson or Swanson, alone or in combination, do not show or suggest the claimed features of the present invention as recited in independent Claims 1 and 9. As such, Applicant also respectfully submits that Ryan and Anderson or Swanson, alone or in combination, do not show or suggest the additional claimed features of the present invention as recited in Claims 2 and 10, and that Claims 2 and 10 are in condition for allowance as being dependent on allowable base claims. As such, the Applicant respectfully asserts that the basis for rejecting Claims 2 and 10 under 35 U.S.C. § 103(a) is traversed.

Claims 4, 12, 17 and 21

The instant Office Action states that Claims 4, 12, 17 and 21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryan in view of

Gorecki (U.S. Patent No. 5,574,678). The Applicant has reviewed the cited references and respectfully submits that the present invention as recited in Claims 4, 12, 17 and 21 is not shown or suggested by Ryan and Gorecki, alone or in combination.

Claim 4 is dependent on Claim 1 and recites additional limitations. Claims 12 is dependent on Claim 9 and recites additional limitations. Claim 21 is dependent on Claim 17 and recites additional limitations. Claim 17 is an independent claim. As presented above, Applicant respectfully submits that Ryan does not show or suggest the present invention as recited in Claims 1, 9 and 17.

Applicant respectfully submits that Gorecki does not overcome the shortcomings of Ryan. Specifically, Applicant respectfully submits that Gorecki, alone or in combination with Ryan, does not show or suggest "A multi-functional device comprising: a bus; a random access memory (RAM) coupled to said bus; a central processing unit (CPU) coupled to said bus; and a plurality of analog blocks coupled to said bus, wherein said bus, RAM, CPU and analog blocks reside on a single chip" as recited in independent Claim 1. Also, Applicant respectfully submits that Gorecki, alone or in combination with Ryan, does not show or suggest "A method for implementing multiple functions in a device, said method comprising selecting a first analog block from a plurality of analog blocks coupled to a bus, a random access memory and a central processing unit on a single chip" as recited in independent Claim 9. Furthermore, Applicant respectfully submits that Gorecki, alone or in combination with Ryan, does

not show or suggest "An array of analog blocks comprising: a first plurality of analog blocks...; and a second plurality of analog blocks ..., and wherein said first plurality and second plurality of analog blocks are coupled to a bus, a random access memory and a central processing unit on a single chip" as recited in independent Claim 17.

Therefore, Applicant respectfully submits that Ryan and Gorecki, alone or in combination, do not show or suggest the claimed features of the present invention as recited in independent Claims 1, 9 and 17, and that these claims are in condition for allowance. As such, Applicant also respectfully submits that Ryan and Gorecki, alone or in combination, do not show or suggest the additional claimed features of the present invention as recited in Claims 4, 12 and 21, and that Claims 4, 12 and 21 are in condition for allowance as being dependent on allowable base claims. As such, the Applicant respectfully asserts that the basis for rejecting Claims 4, 12, 17 and 21 under 35 U.S.C. § 103(a) is traversed.

Conclusions

In light of the above remarks, Applicant respectfully requests reconsideration of the rejected claims.

Based on the arguments presented above, Applicant respectfully asserts that Claims 1-22 overcome the rejections of record and, therefore, Applicant respectfully solicits allowance of these claims.

The references cited but not relied upon have been reviewed. These references were not found to show or suggest the present claimed invention: U.S. Patent Nos. 6,614,260 and 6,003,054.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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